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Applicant(s): T. WAKABAYASHI

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For : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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Examiner : Luan C. Thai

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EXPEDITED PROCEDURE
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Yolanda Usher
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RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE - GROUP 2827

Commissioner for Patents
Washington, D.C. 20231

S I R :

This is responsive to the Final Office Action mailed July 31, 2002, the term for response to which expires on October 31, 2002.

IN THE CLAIMS

Please cancel claims 31-33 without prejudice, and substitute amended claims 17, 21, 26, 29 and 35 as follows:

17. (Amended) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip-forming regions, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench successively extending to half a thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a first seal film on the upper surface of the semiconductor wafer in a manner such that the trenches are filled and such that a top surface of each of the outer connection terminals is exposed;

forming a second seal film on the lower surface of the semiconductor wafer; and

cutting the first seal film along the trenches by removing parts of the first seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual semiconductor devices, each of which has the first seal film provided on an upper surface thereof and on an upper part of a periphery thereof while leaving a lower part of the periphery thereof exposed, and each of which has the second seal film provided on the lower surface thereof.

21. (Amended) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip-forming regions, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface;

forming a rear seal film on the lower surface of the semiconductor wafer;

adhering a dicing tape to a lower surface of the second seal film;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench successively extending from the upper surface of the semiconductor wafer to half a thickness of the dicing tape so as to form concavities in an upper portion of the dicing tape;

forming a front seal film on the upper surface of the semiconductor wafer in a manner such that the trenches are filled and such that a top surface of each of the outer connection terminals is exposed; and

cutting the front seal film along the trenches by removing parts of the front seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual semiconductor devices, each of which has the front seal film provided on an upper surface thereof and on an entire

surface of a periphery thereof, and each of which has the rear seal film provided on the lower surface thereof.

26. (Amended) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip forming regions, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of connection pads formed on the upper surface;

forming on the upper surface of the semiconductor wafer an insulating film having openings such that the upper surface of the semiconductor wafer is covered and the connection pads are exposed via the openings;

forming on the insulating film wirings connected to the connection pads;

forming pillar-shaped electrodes on the wirings;

adhering a dicing tape to the lower surface of the semiconductor wafer;

making trenches in parts of the semiconductor wafer which lie between the chip-forming regions, each trench successively extending from the upper surface of the semiconductor wafer to half a thickness of the dicing tape so as to form concavities in an upper portion of the dicing tape;

forming a seal film on the upper surface of the semiconductor wafer in a manner such that the trenches are filled

and such that a top surface of each of the pillar-shaped electrodes is exposed; and

cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual semiconductor devices, each of which has the seal film provided on an upper surface thereof and on a periphery thereof, wherein a portion of the seal film provided on the periphery projects from a lower surface of the semiconductor devices.

29. (Amended) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip forming regions, a lower surface opposing the upper surface, a thickness between the upper and lower surfaces, and a plurality of pillar-shaped electrodes formed on the upper surface;

adhering a dicing tape to the lower surface of the semiconductor wafer;

making trenches by cutting parts of the semiconductor wafer which lie between the chip-forming regions, each trench successively extending to half a thickness of the dicing tape through the thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a seal film on the upper surface of the semiconductor wafer so as to fill in the trenches and cover the pillar-shaped electrodes;

polishing an upper surface of the seal film until a top surface of each of the pillar-shaped electrodes is exposed;

cutting the seal film along the trenches by removing parts of the seal film having a smaller width than the trenches;

adhering a support tape to the upper surface of the seal film after cutting the seal film along the trenches;

peeling off the dicing tape from the lower surface of the semiconductor wafer after adhering the support tape to the upper surface of the seal film, and

polishing the lower surface of the semiconductor wafer after peeling off the dicing tape.

35. (Amended) A method of manufacturing a semiconductor device comprising:

preparing a semiconductor wafer having an upper surface including chip forming regions, a lower surface opposing the upper surface, a thickness between the upper and lower surfaces, and a plurality of pillar-shaped electrodes formed on the upper surface;

forming a rear seal film on the lower surface of the semiconductor wafer;

making trenches by cutting in parts of the semiconductor wafer which lie between the chip-forming regions, each trench

successively extending to half a thickness of the rear seal film through the a thickness of the semiconductor wafer from the upper surface of the semiconductor wafer;

forming a front seal film on the upper surface of the semiconductor wafer so as to cover the upper surface of the semiconductor wafer while leaving a top surface of each of the pillar-shaped electrodes exposed, and so as to fill in the trenches and thereby entirely enclose each of the chip-forming regions within the front seal film and the rear seal film; and

cutting the front seal film along the trenches by removing parts of the front seal film having a smaller width than the trenches such that the semiconductor wafer is separated into individual devices, each of which has the front seal film provided on the upper surface thereof and on a periphery thereof, and each of which has the rear seal film provided on the lower surface thereof.

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

ALLOWABLE SUBJECT MATTER

The Examiner's indication of the allowability of the subject matter of claims 21-23 is respectfully acknowledged.

Allowable claim 21 has been rewritten in independent form to include all of the limitations of claims 17 and 18 from which claim 21 formerly depended. Accordingly, it is respectfully submitted that amended claim 21 and claims 22 and 23 depending therefrom are now in condition for immediate allowance.

THE REJECTED CLAIMS

The rejection of claims 17-20, 24 and 25, and the rejections of claims 26-28, 29-34 and 35-37 are respectfully traversed as follows with respect to independent claims 17, 26, 29 and 35 as amended hereinabove.

Claims 17-20, 24 and 25

According to the present invention as recited in amended claim 17, a method of manufacturing a semiconductor device is provided which comprises the steps of:

(a) making trenches so as to successively extend to half a thickness of a wafer;

(b) forming a first seal film on the upper surface of the wafer and a second seal film on the lower surface of the wafer; and

(c) cutting the first seal film such that the wafer is separated into individual semiconductor devices, each of which has the first seal film provided on the upper surface thereof and on an upper part of a periphery thereof while leaving a lower part of the periphery thereof exposed, and each of which has the second seal film provided on the lower surface thereof.

Original claim 17 was rejected under 35 USC 103 as being obvious in view of the combination of USP 5,989,982 ("Yoshikazu") and USP 6,287,893 ("Elenius et al").

As recognized by the Examiner, Yoshikazu discloses in Figs. 2B and 2C making trenches in a wafer. It is respectfully submitted, however, that Fig. 2C of Yoshikazu clearly shows that the trenches thereof do not extend to half a thickness of the wafer, as according to the present invention as recited in claim 17.

As also recognized by the Examiner, Yoshikazu discloses in Figs. 2G and 2H cutting a first seal film provided on the upper surface of the wafer such that the wafer is separated into individual devices, each of which has the first seal film provided on the upper surface of the wafer. It is respectfully submitted, however, that Yoshikazu does not disclose, teach or suggest that each of the individual devices have the first seal film provided on an upper part of a periphery thereof while

leaving a lower part of the periphery thereof exposed, and a second seal film provided on the lower surface thereof.

Accordingly, it is respectfully submitted that Yoshikazu does not at all disclose, teach or suggest the above described features (a), (b) and (c) of the present invention as recited in amended claim 17.

Elenius discloses in Fig. 2 thereof cutting of a seal film such that a wafer is separated into individual devices, each of which has a first seal film on a upper surface of the wafer and a second seal film on a lower surface of the wafer. It is respectfully submitted, however, that according to the teachings of Elenius, the periphery of each of individual devices is exposed and is <u>not</u> covered with a seal film.

Accordingly, it is respectfully submitted that Elenius fails to disclose, teach or suggest the above described feature (c) of the present invention as recited in amended claim 17. (And it is also noted that Elenius also fails to disclose, teach or suggest the above described feature (a) of the present invention as recited in amended claim 17.)

In addition, it is also noted that although USP 6,107,164 ("Ohuchi") discloses in Fig. 3C and Fig. 3D thereof the making of trenches (grooves) in a wafer so as to extend to half a thickness of the wafer from an upper surface of the wafer, this reference nevertheless discloses at column 3, lines 36 to 53 that the grooves 22 thereof are exposed by cutting away from the back of the wafer. (See Figs. 4A to 4C of Ohuchi.) Therefore, in

Ohuchi, the entire surface of the periphery of the individual devices is covered by the seal film - and the lower surface of the individual devices is not covered by the seal film. Thus, it is respectfully submitted that Ohuchi also does not disclose, teach or suggest the above described features (b) and (c) of the present invention as recited in claim 17.

In view of the foregoing, it is respectfully submitted that claim 17 as well as each of claims 18-20, 24 and 25 depending therefrom all patentably distinguish over any combination of the cited references under 35 USC 103.

Claims 26-28

According to the present invention as recited in amended claim 26, a method of manufacturing a semiconductor device is provided which comprises the steps of:

(d) adhering a dicing tape to a lower surface of a wafer on which pillar-shaped electrodes are formed;

(e) making trenches in the wafer so as to successively extend to half a thickness of the dicing tape so as to form concavities in an upper portion of the dicing tape; and

(f) cutting the seal film such that the wafer is separated into individual devices, each of which has the seal film provided on the upper surface thereof and on a periphery thereof, wherein a portion of the seal film provided on the periphery projects from a lower surface of the semiconductor devices.

Yoshikazu discloses in Figs. 2A to 2C adhering of a dicing tape to the lower surface of a wafer on which pillar-shaped electrodes are formed, and making of trenches in the wafer. It is respectfully pointed out, however, that the trenches in the wafer of Yoshikazu do not extend to half a thickness of the dicing tape so as to form concavities in the upper portion of the dicing tape, as according to the present invention as recited in amended claim 26.

In addition, it is respectfully pointed out that as can be seen in Fig. 2 of Yoshikazu, a portion of the seal film provided on the periphery of an individual device is not projected from a lower surface of the individual device.

Accordingly, it is respectfully submitted that Yoshikazu does not disclose, teach or suggest the above described features (e) and (f) of the present invention as recited in amended claim 26.

Elenius, moreover, makes no mention of a dicing tape, and Fig. 2 of Elenius illustrates that a seal film is not provided on a periphery. Accordingly, it is respectfully submitted that Elenius fails to disclose, teach or suggest the above described features (d) and (f) of the present invention as recited in amended claim 26.

Still further, it is respectfully pointed out that USP 6,159,837 ("Yamaji et al") also makes no mention of a dicing tape, and does not disclose, teach or suggest providing a seal film on a periphery.

In view of the foregoing, it is respectfully submitted that claim 26 as well as each of claims 27 and 28 depending therefrom all patentably distinguish over any combination of the cited references under 35 USC 103.

Claims 29-34

According to the present invention as recited in amended claim 29, a method of manufacturing a semiconductor device is provided which comprises the steps of:

(g) adhering a dicing tape to the lower surface of a wafer and making trenches by cutting so as to successively extend to half a thickness of the dicing tape;

(h) adhering a support tape to the upper surface of a seal film, polishing an upper surface of the seal film, and then cutting the seal film;

(i) peeling off the dicing tape from the lower surface of the wafer after adhering the support tape; and

(j) polishing the lower surface of the wafer after peeling off the dicing tape.

Yoshikazu discloses in Figs. 2A to 2C adhering of a dicing tape to the lower surface of the wafer, and making trenches in the wafer. As noted above, however, it is respectfully pointed out that the trenches in the wafer of Yoshikazu do not extend to half a thickness of the dicing tape, as according to the present invention as recited in amended claim 26.

In addition, it is respectfully pointed out that Yoshikazu makes no mention of a support tape.

Accordingly, it is respectfully submitted that Yoshikazu does not disclose, teach or suggest the above described features (h), (i) and (j) of the present invention as recited in amended claim 29.

With respect to Ohuchi, it is noted that this reference appears to illustrate in Figs. 3A to 3D and Figs. 4A to 4C the making of trenches in a wafer on which pillar-shaped electrodes are formed so as to extend to half a thickness of the wafer. In Ohuchi, however, a dicing tape is not used, and it is clear that each of the trenches does not extend to the dicing tape. In addition, it is respectfully pointed out that this reference makes no mention of a support tape.

Accordingly, it is respectfully submitted that Ohuchi does not disclose, teach or suggest the above described features (g), (h) and (i) of the present invention as recited in amended claim 29.

With respect to Ohuchi, moreover, it is noted that this reference discloses at column 7, lines 2-4 that "When the bottom side of the wafer 21 has been lapped as far as the grooves 22, the wafer is divided into chips 29." As is clear from this statement, in Ohuchi the sheet 9 is required to fix the wafer when the wafer is diced into chips. Thus, the sheet 9 is merely a counterpart to the scribe sheet 7 of Yoshikazu in terms of function.

Still further, it is noted that although USP 5,888,883 ("Sasaki") illustrates in Figs. 10 and 11 thereof adhering a support tape on an upper surface of a seal film after making trenches in a wafer (column 6, line 54 to column 7, line 15), the trenches in this reference are terminated at a halfway point in a thickness of the wafer. And it is also noted that there is no disclosure in this reference of a dicing tape.

In view of the foregoing, it is respectfully submitted that claim 29 as well as each of claims 30-34 depending therefrom all patentably distinguish over any combination of the cited references under 35 USC 103.

Claims 35 and 36

According to the present invention as recited in amended claim 35, a method of manufacturing a semiconductor device is provided which comprises the steps of:

(k) making trenches by cutting to form trenches which each extend to half a thickness of a rear seal film formed on the lower surface of a wafer;

(l) forming a front seal film on the upper surface of the wafer so as to fill in the trenches and thereby entirely enclose each of chip-forming regions within the front seal film and the rear seal film; and

(m) cutting the seal film such that the wafer is separated into individual devices, each of which has the front seal film, provided on an upper surface thereof and on a periphery thereof,

and each of which has the rear seal film provided on the lower surface thereof.

Yoshikazu makes no mention of a rear seal film and therefore does not disclose, teach or suggest any of the above features (k), (l) and (m) of the present invention as recited in amended claim 35.

And although Elenius does disclose the use of a rear seal film, it is respectfully submitted that this reference does not disclose, teach or suggest forming each trench to extend to half a thickness of the rear seal film, as according to the present invention as recited in amended claim 35.

In addition, Elenius also does not disclose, teach or suggest that a seal film is formed at a periphery.

Accordingly, Elenius, like Yoshikazu, does not disclose, teach or suggest any of the above features (k), (l) and (m) of the present invention as recited in amended claim 35.

In view of the foregoing, it is respectfully submitted that claim 35 as well as claim 36 depending therefrom both patentably distinguish over any combination of the cited references under 35 USC 103.

CLAIM FEE

The application formerly contained 21 claims of which 4 were independent, and the appropriate claim fee was paid for such claims. The application now contains 18 claims, of which 5 are independent. Accordingly, a claim fee in the amount of $84.00

for the addition of 1 extra independent claim is attached hereto. In addition, authorization is hereby given to charge any additional fees which may be determined to be required to Account No. 06-1378.

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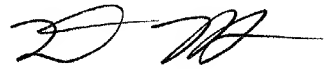
In view of the foregoing, entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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